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Amendments to the Claims

Please amend the claims as shown below. This listing of Claims replaces all prior versions and listings of the claims in this application.

Listing of Claims

1. (Currently Amended) A method for fabricating an RF semiconductor device comprising:

forming a trench to define an active region and an element isolation region in a semiconductor substrate;

forming a plurality of gate lines within the active region of the semiconductor substrate, the plurality of gate lines running perpendicularly to the trench and not extending over a center of the trench;

forming an insulating layer on the plurality of gate lines and the semiconductor substrate;

forming ~~all~~ contact holes in the insulating layer over the active region using a single pattern, wherein a first group of the contact holes exposes portions of the gate lines and a second group of the contact holes exposes portions of the substrate in the active region;

forming contact plugs in each of the contact holes; and

forming a conductive pattern layer over the insulating layer that is electrically connected with the contact plugs.

2. (Previously Presented) A method as defined in claim 1, wherein the gate lines are not connected with each other in the element isolation region.

3. (Previously Presented) A method as defined in claim 1, wherein at least two of the plurality of gate lines are connected in the active region.

4. (Original) A method as defined in claim 1, wherein a thickness of the insulating layer is about 1000 to about 20000 angstroms.

5. (Original) A method as defined in claim 1, wherein a thickness of the conductive pattern layer is above 10000 angstroms.

6. (Previously Presented) A method as defined in claim 1, wherein the insulating layer comprises an oxide or a polyimide.

7. (Currently Amended) A method as defined in claim 1, wherein forming the plurality of gate lines minimizes parasitic capacitance between the plurality of gate lines and the substrate.

8. (Previously Presented) A method as defined in claim 1, wherein forming the plurality of gate lines minimizes resistance of the plurality of gate lines.

9. (Previously Presented) A method as defined in claim 1, further comprising metal contacts linking at least two of the plurality of gate lines.

10. (Previously Presented) A method as defined in claim 1, wherein the plurality of gate lines do not extend along a longitudinal axis of the trench.

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Previously Presented) A method as defined in claim 1, wherein adjacent gate lines are formed at a substantially constant distance along their lengths.

16. (Previously Presented) A method as defined in claim 1, wherein the second group of contact holes are formed between the plurality of gate lines.

17. (Previously Presented) A method as defined in claim 1, wherein the element isolation region comprises the trench.

18. (Previously Presented) A method as defined in claim 1, wherein forming the contact plugs comprises:

forming a first conductive layer over the insulating layer and in the contact holes; and

planarizing the first conductive layer.

19. (Previously Presented) A method as defined in claim 18, wherein planarizing the first conductive layer exposes an upper surface of the insulating layer.

20. (Previously Presented) A method as defined in claim 1, wherein the insulating layer comprises a low temperature oxide.

21. (Canceled)

22. (Currently Amended) A method as defined in claim [[21]]1, wherein the plurality of gate lines do not extend longitudinally along a longitudinal axis of the trench.

23. (Currently Amended) A method as defined in claim [[22]]1, wherein the plurality of gate lines do not extend horizontally along a longitudinal axis of the trench.